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Claims

What is claimed is:

1. A test circuit for a device, comprising:

a test vector decode circuit configured to receive at least one input signal, including a drive maintenance signal, and a latch enable signal, said test vector decode circuit further configured to transmit at least one output signal to said device responsive to said latch enable signal, including a lockout signal further responsive to a reception of said drive maintenance signal; and

a test vector recognition circuit coupled to said test vector decode circuit and configured to transmit said latch enable signal in response to a reception of a latch prompt signal, and said test vector recognition circuit further configured to receive said lockout signal and overridingly exclude said latch enable signal responsive to said lockout signal.

2. The test circuit in claim 1, wherein said test circuit further comprises a reset circuit coupled to said test vector decode circuit and configured to reset said lockout signal in response to a reception of a reset prompt signal.

3. A test mode regulation device for a decode circuit coupled to a plurality of address input pathways, a reset signal pathway, and a plurality of test vector output pathways, and

further configured to receive a latch enable pathway and perform at least one decode circuit operation, comprising:

an additional test vector output pathway configured to couple to said decode circuit and further configured to transmit a disable signal in response to a final decode circuit operation; and

a logic unit configured to electrically interpose between said latch enable pathway and said decode circuit, wherein said logic unit comprises:

a first input coupled to said latch enable pathway,

a second input coupled to said additional test vector output pathway, and

an output coupled to said decode circuit,

and said logic unit configured to prevent a drive communication between said latch enable pathway and said decode circuit in response to said disable signal.

4. The test mode regulation device in claim 3, wherein said final decode circuit operation comprises a logic function performed on at least one signal from said plurality of address input pathways.

5. The test mode regulation device in claim 4, said additional test vector output pathway further configured to transmit an enable signal in response to a reset transmission from said reset signal pathway; and said logic unit configured to reestablish said drive communication between said latch enable pathway and said decode circuit in response to said enable signal.

6. The test mode regulation device in claim 5, wherein said logic unit is an OR gate.

7. A test device, comprising:

a test vector decode circuit;

an output node coupled to said decode circuit; and

a lockout device coupled to said decode circuit and configured to decouple said decode circuit from said output node after an operation of said decode circuit.

8. The test device in claim 7, said lockout device configured to decouple said output node in response to said operation of said decode circuit.

9. A test vector decode circuit comprising:

a logic circuit;

at least one input terminal coupled to said logic circuit;

a latch terminal coupled to said logic circuit;

at least one output terminal coupled to said logic circuit; and

a latch disabling device coupled to said output terminal and to said latch terminal,

said latch disabling device configured to activate in response to an output vector from said output terminal, and

said output terminal configured to transmit said output vector in response to a combination of:

an input signal received at said input terminal, and

a logic circuit operation.

10. The test vector decode circuit in claim 9, further comprising a reset terminal coupled to said internal logic circuit and configured to transmit a deactivation signal to said latch disabling device through said internal logic circuit in response to a reset signal received at said reset terminal.

11. A test circuit comprising:

a test vector decode device;

an input node coupled to said test vector decode device;

an output node coupled to said test vector decode device;

a latch node; and

a latch device coupled to said latch node and configured to receive a latch prompt signal and further configured to alternatively receive an initial signal and an anti-latch signal, said latch device further configured to allow electrical communication between said input node and said output node in response to a combination of said initial signal and said latch prompt signal and to prevent said electrical communication in response to said anti-latch signal.

12. The circuit in claim 11, said input node configured to receive a test-mode-end signal, said output node is coupled to said latch device, and said output node configured to transmit said initial signal and to alternatively transmit said anti-latch signal in response to:

a reception of said test-mode-end signal by said input node; and

a reception of said latch prompt signal by said latch device.

13. The circuit in claim 12, said output node further configured to couple to an external device.

14. The circuit in claim 13, said output node configured to receive a signal maintaining voltage source.

15. A test decode system comprising:

a decode circuit, further comprising an output node configured to send at least one test drive transmission, including a last test drive transmission; and

a latch device coupled to said decode circuit and configured to allow electrical communication within said decode circuit, and further configured to deactivate generally concurrently with said last test drive transmission from said output node.

16. The test decode system in claim 15, said latch device coupled to said output node and further configured to deactivate responsive to said last test drive transmission.

17. A lockout device for a decode circuit having at least one decode function, including a test-mode-completion decode function comprising:

a latch control terminal configured to couple to said decode circuit and further configured to alternatively transmit:

a lockout signal in response to said test-mode-completion decode function of said decode circuit, and

an admission signal; and

a logic circuit, further comprising:

an output terminal configured to couple to said decode circuit,

a first input terminal configured to receive a decode initiation signal,

said logic circuit configured to initiate said decode function responsive to said decode initiation signal, and

a second input terminal coupled to said latch control terminal and further configured to prevent said decode function responsive to said lockout signal.

18. The device in claim 17, further comprising a mode shifter configured to couple to said decode circuit, said mode shifter configured to transmit a reset signal in response to an external signal; and said latch control terminal configured to send said admission signal generally responsive to said reset signal.

19. The device in claim 18, said latch control terminal configured to retransmit said admission signal exclusively in response to said reset signal.

20. The device in claim 19, said mode shifter configured to couple to said latch control terminal through said decode circuit.

21. The device in claim 20, said mode shifter further configured to transmit a non-reset signal absent said external signal; and said decode circuit configured to receive a voltage source having a first magnitude, and said non-reset signal has a voltage with a second magnitude greater than said first magnitude.

22. The device in claim 21, said non-reset signal is a supervoltage signal.

23. A signal maintainer for an operations circuit configured to receive at least one input, perform a function on said input in response to a reception of a function prompt signal, and transmit at least one output, comprising:

a lockout circuit configured to couple to said operations circuit, to carry said function prompt signal to said operations circuit, and to receive a lockout signal, and said lockout circuit further configured to selectively block any function prompt signal in response to a reception of said lockout signal and to alternatively carry any function prompt signal to said operations circuit;

an electrical communication component coupled to said lockout circuit and configured to carry said lockout signal.

24. The signal maintainer in claim 23, said electrical communication component configured to further couple to said operations circuit and to carry an output of said operations device to said lockout circuit.

25. The signal maintainer in claim 24, said lockout circuit further configured to receive a reset prompt signal and refrain from blocking said function prompt signal in response to a reception of said reset prompt signal.

26. The signal maintainer in claim 25, said electrical communication component further configured to carry said reset prompt signal to said lockout circuit.

27. A latch regulator for a circuit, comprising:

a lockout pathway configured to carry a disable signal having a first value and a second value; and

a logic apparatus having:

a first input node coupled to said lockout pathway,

a second input node configured to receive a latch prompt signal, and

an output node configured to couple to said circuit,

and said logic apparatus configured to recognize a change in said latch prompt signal while said disable signal has said first value and further configured to disregard said change in said latch prompt signal while said disable signal has said second value.

28. The latch regulator in claim 27, said logic apparatus further configured to transmit a latch enable signal to said circuit in recognition of said change in said latch prompt signal.

29. The latch regulator in claim 28, said lockout pathway configured to couple to an output terminal of said circuit and further configured to initially carry said disable signal having said first value and to subsequently carry said disable signal having said second value in response to a latching of an input for said circuit.

30. The latch regulator of claim 29, said lockout pathway further configured to carry said disable signal having said first value in response to a reset transmission to said circuit.

31. The latch regulator of claim 29, said logic apparatus comprising a NOR gate.

32. The latch regulator of claim 29, said logic apparatus comprising an AND gate.

33. The latch regulator of claim 29, said logic apparatus comprising a NAND gate.

34. A method for regulating the ability of a testing circuit to latch output vectors, comprising:

latching only in response to changing at least one output vector; and

allowing a change in said output vector only in response to latching and to resetting said output vector.

35. A method for regulating the ability of a testing circuit to latch at least one output vector, comprising:

designating one output veetor as a lockout vector;

allowing at least one latching;

associating at least one latching with a first change of said lockout vector;

initiating said first change of said lockout vector;

allowing further latching only in response to a second change of said lockout vector; and

allowing said second change in lockout vector only in response to further latching and to resetting said lockout vector.

36. The method in claim 35, wherein:

said method further comprises establishing an initial value for said lockout vector;

initiating said first change of said lockout vector further comprises changing said initial value of said lockout vector; and

allowing further latching comprises allowing further latching only in response to a restoration of said initial value.

37. A method of preventing a circuit having a test mode entry function from entering a subsequent test mode after said circuit enters a first test mode, comprising:

initiating a test mode blocking signal after said circuit completes said first test mode; and

exclusively controlling said test mode entry function of said circuit with said test mode blocking signal.

38. The method in claim 37, further comprising generating said test mode blocking signal responsive to a final test latch of said circuit during said first test mode.

39. The method in claim 38, further comprising originating said test mode blocking signal from said circuit.

40. A method of preserving a state of an output of a test vector decode circuit, said test vector decode circuit configured to change said state of said output in response to receiving a latch signal, comprising:

producing a blocking signal; and

isolating said circuit from any latch signal with said blocking signal.

41. The method of claim 40, further comprising transmitting said blocking signal as an output of said circuit.

42. A method of testing a circuit, comprising:

receiving at least one address input;

receiving at least one latching signal;

performing a decoding operation on each address input;

transmitting a result of said decoding operation as at least one output test vector in response to each latching signal;

driving said circuit with each output test vector;

generating a latch prevention signal; and

overriding any subsequent latching signal with said latch prevention signal.

43. The method in claim 42, wherein generating comprises generating said latch prevention signal in response to transmitting a result of a decoding operation.

44. The method in claim 43, further comprising enabling said latch prevention signal to be overridden.

45. A method of sustaining a potential of a signal from an output pathway of a test vector decode device coupled to a logic circuit, said logic circuit configured to carry a potential-changing transmission to said test vector decode device, comprising:

maintaining a state of electrical communication between said logic circuit and said test vector decode device; and

preventing further changes in said state of electrical communication between said logic circuit and said test vector decode device.

46. A method for testing an external circuit, comprising:

subjecting an address input to a logic function;

generating an output vector;

driving said external circuit with said output vector;

generating a lockout signal; and

prohibiting subjecting an address input to a logic function during a generation of said lockout signal.

47. A method of regulating the value of a test signal, comprising:

initiating a latch mode;

accepting an input signal;

performing a logic operation on said input signal;

deriving an output signal; and

initiating an input lockout mode.

48. The method in claim 47, further comprising deriving a plurality of output signals, and wherein initiating an input lockout mode comprises initiating said input lockout mode with one output signal of said plurality of output signals.

49. The method in claim 48, further comprising reestablishing said latch mode through a reset signal.

50. The method in claim 49, further comprising reestablishing said latch mode exclusively through said reset signal.

51. The method in claim 50, wherein reestablishing said latch mode through said reset signal comprises resetting said one output signal that initiated said input lockout mode.

52. A method of protecting a test circuit from receiving a subsequent latching signal after receiving at least one prior latching signal, comprising:

allowing at least one prior latching signal to reach said test circuit;

performing a test circuit operation for each prior latching signal;

providing a lockout signal; and

stopping any subsequent latching signal with said lockout signal.

53. The method in claim 52, wherein providing said lockout signal further comprises generating said lockout signal responsive to a last prior latching signal.

54. A method of preventing a test vector decode circuit from reentering a test mode, comprising:

making a reentry into said test mode dependent upon a change of an output vector of said test vector decode circuit; and

making said change of said output vector dependent upon said reentry into said test mode.